Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.058”**

**PAD FUNCTION:**

1. **VDD**
2. **DB**
3. **S8**
4. **S7**
5. **S6**
6. **S5**
7. **S4**
8. **S3**
9. **S2**
10. **S1**
11. **GND**
12. **N/C**
13. **A2**
14. **A1**
15. **AO**
16. **EN**
17. **S1**
18. **S2**
19. **S3**
20. **S4**
21. **S5**
22. **S6**
23. **S7**
24. **S8**
25. **VSS**
26. **DA**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**11**

**2 1 26**

**25**

**24**

**23**

**22**

**21**

**20**

**19**

**18**

**17**

**12 13 14 15 16**

**.116”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” x .004” min.**

**Backside Potential: NC**

**Mask Ref: AD3600**

**APPROVED BY: DK DIE SIZE .058” X .116” DATE: 6/16/22**

**MFG: ANALOG DEVICES THICKNESS .014” P/N: ADG507A**

**DG 10.1.2**

#### Rev B, 7/19/02